Intel Pentium

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Additional Versions

- Celeron processor is a discount version of the Pentium.
- Xeon is a high end version of the Pentium.
- Pentium M is designed for mobile systems
- Itanium is a RISC processor
- MMX™ Technology was added for multimedia.
  - Intel makes several other processors

Transistors

- The original 8086 had 29K transistors on the processor die.
- A Pentium 4 with HT has 125M transistors
- A Pentium M processor as 140M transistors

Compatibility

- Intel has maintained compatibility through the entire line.
- A program compiled for a 8086 will run on a Pentium 4 or Itanium processor.
- The desire for compatibility has limited the ability to change the processor design.

X86 History

<table>
<thead>
<tr>
<th>Processor</th>
<th>Year</th>
<th>Freq (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4004</td>
<td>1971</td>
<td></td>
</tr>
<tr>
<td>8088</td>
<td>1978</td>
<td>4.77</td>
</tr>
<tr>
<td>8086</td>
<td>1979</td>
<td>8</td>
</tr>
<tr>
<td>80286</td>
<td>1982</td>
<td>12.5</td>
</tr>
<tr>
<td>80386</td>
<td>1985</td>
<td>20</td>
</tr>
<tr>
<td>80486</td>
<td>1989</td>
<td>25</td>
</tr>
<tr>
<td>Pentium</td>
<td>1993</td>
<td>60</td>
</tr>
<tr>
<td>Pentium Pro</td>
<td>1995</td>
<td>200</td>
</tr>
<tr>
<td>Pentium II</td>
<td>1997</td>
<td>266</td>
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<td>Pentium III</td>
<td>1999</td>
<td>500</td>
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<td>Pentium 4</td>
<td>2000</td>
<td>1500</td>
</tr>
<tr>
<td>Pentium 4 Ex</td>
<td>2004</td>
<td>3060</td>
</tr>
</tbody>
</table>

8080 Hand Drawn Chip Layout
Processor Modes

- Pentium supports two modes
  - Real mode
    • Uses 16-bit addresses
    • Runs 8086 programs
    • Pentium acts as a faster 8086
  - Protected mode
    • Supports memory protection
    • 32-bit mode
    • Native mode of Pentium
    • Supports segmentation and paging

Registers

- General-Purpose Registers
  - Eight 32-bit Registers
  - Six 16-bit Registers
  - Eight 80-bit Registers

Segment Registers

- 32-bits
- BPL/OS Register
- EIP (Instruction Pointer Register)

FPU Registers

- 80-bits
- Floating-Point Data Registers

Extended Register Use

- 32-bit registers

<table>
<thead>
<tr>
<th>32-bit registers</th>
<th>16-bit registers</th>
<th>8-bit registers</th>
<th>0-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>AH</td>
<td>AL</td>
<td>A</td>
</tr>
<tr>
<td>EBX</td>
<td>BH</td>
<td>BL</td>
<td>BX</td>
</tr>
<tr>
<td>ECX</td>
<td>CH</td>
<td>CL</td>
<td>CX</td>
</tr>
<tr>
<td>EDX</td>
<td>DH</td>
<td>DL</td>
<td>DX</td>
</tr>
</tbody>
</table>

Segmented Memory

- Segment Registers
- Code Segment
- Stack Segment
- Data Segment
- Data Segment
- Data Segment

Segment Overlap

- (a) Adjacent
- (b) Disjoint
- (c) Partially overlapped
- (d) Fully overlapped

Real Mode Addressing

- Real mode physical addresses are 20 bits
- A 16 bit segment pointer contains the start address of a segment.
- An instruction can contain a 16 bit offset.
- The segment address is shifted left 4 bits and added to the offset.

1234h segment pointer
3333h offset
15673h physical address
Intel Pentium Architecture

Protected Mode Segment Addresses

- Segment table
- Page table
- Physical Addr

Protected Mode Segment Addresses

<table>
<thead>
<tr>
<th>Segment</th>
<th>Page</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 bits</td>
<td>10 bits</td>
<td>12 bits</td>
</tr>
</tbody>
</table>

- EFLAGS Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>30-23</td>
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<tr>
<td>22-19</td>
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</tr>
<tr>
<td>18-15</td>
<td></td>
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<tr>
<td>14-11</td>
<td></td>
</tr>
<tr>
<td>10-0</td>
<td></td>
</tr>
</tbody>
</table>

RISC-Like Architecture

- The Pentium has two execution engines, one for simple instructions and the other for all instructions.
- The simple execution engine runs a subset of the instructions. This is optimized for fast execution.
- Complex instructions are executed by another execution engine.

Out-Of-Order Execution

- The Pentium 4 can execute instructions out of sequential order if there are no hazards.

MMX™ Technology

- Multimedia Extensions (MMX) is a set of new instructions introduced to aid video and audio processing.
- They perform single-instruction multiple-data (SIMD) operations.
- Perform parallel operations on packed integers in the floating point registers.
- Floating point registers used for compatibility.

Hyper-Threading Technology

- Enables a single physical processor to execute two separate code streams (threads) concurrently.
- Each logical processor has its own set of registers.
- Logical processors share the core resources of the physical processor including the execution engine and the system bus.