I/O Controllers

COMP375 Computer Architecture and Organization

I/O Controllers

Internal & External

- The CPU, memory and bus are internal components of a computer.
- Everything else is an input or output device.

I/O Devices

<table>
<thead>
<tr>
<th>Disk</th>
<th>Keyboard</th>
</tr>
</thead>
<tbody>
<tr>
<td>hard</td>
<td>Speakers</td>
</tr>
<tr>
<td>floppy</td>
<td>Printer</td>
</tr>
<tr>
<td>CD</td>
<td>Mouse</td>
</tr>
<tr>
<td>DVD</td>
<td>Scanner</td>
</tr>
<tr>
<td>Monitor</td>
<td>Game controller</td>
</tr>
<tr>
<td>Network</td>
<td>USB drive</td>
</tr>
</tbody>
</table>

Many, many more

Device Speed

![Graph from Stallings textbook]
Many Different Devices

- I/O devices differ in
  - Speed
  - Granularity
  - Control
- I/O controllers interface between the many different devices and the internal system components; CPU, memory and bus

Basic Computer Components

Processor’s View Of I/O

- A processor does not access external devices directly.
- Instead, the processor uses a programming interface to pass requests to an I/O controller, which translates the requests into the appropriate external signals.
I/O Controller

- Connects the I/O devices to the system.
- Communicates with the CPU and the RAM over the bus.
- A single I/O controller may control multiple devices.
- Most computers have several I/O controllers.
- Actions are initiated by the CPU.

I/O Controller Functionality

- Interface translation
  - connection, voltage
  - protocol
  - clocking
- Addressing
- Multiplexing
- Buffering
- Error detection and correction
- Control of multiple steps

How many I/O controllers do most computers have?

1. 1
2. 3
3. 1 for each device
4. 1 for each type of device
5. 3 for each device

I/O Addressing

- The CPU communicates with the I/O controllers over the bus using the same fetch and store protocol as memory.
- Each I/O controller has a unique address, possibly several addresses.
- I/O addresses can be
  - independent of memory addresses
  - in the same as memory, but not overlapping with memory. This is memory mapped I/O.
I/O Controllers

I/O Address Range
• Some systems have a separate address space for program data and instructions and another address space for I/O devices.

Memory Mapped I/O
• Some systems use the same address space for memory and I/O devices.

Control And Status Registers
• An I/O controller addresses provide
  – Data transfer
  – Control
    • Device address
    • Read or Write or other operation
  – Status
    • Device ready
    • Operation complete
  • Respond to *fetch* or *store* operation

Example I/O
```
checkio LOAD R1, DeviceStatus
AND R1, IOreadyBit
JZ checkio
LOAD R2, databyte
STORE R2, DeviceData
```

- **DeviceStatus**: addr of I/O status register
- **IOreadyBit**: bit indicating device ready
- **DeviceData**: addr of I/O data register
Buffering

- Some I/O controllers store and analyze incoming data in controller memory.
- An Ethernet controller will receive the data into local memory on the controller card. The data will only be transferred to RAM if it was received correctly and has the machine address.
- Controllers may perform many transformations on the data.

Compared to the speed of the bus, most I/O devices are

1. Faster
2. Slower
3. Same speed
4. None of the above

Latency And Throughput

- The latency of an interface is a measure of the time required to perform a transfer.
- The throughput of an interface is a measure of the data that can be transferred per unit time.

Multiple Step Control

- Operating a device may involve many separate steps. An I/O controller can specify the individual steps to a device to carry out a function specified by the CPU.
- The controller can detect errors in the operation of a device. It may also attempt to recover from errors.
I/O Controllers

Dumb Controller Example
• Processor performs all the work
• Example of interaction
  – Processor starts the disk spinning
  – Disk interrupts when it reaches full speed
  – Processor starts disk arm moving to the desired location
  – Disk interrupts when arm is in position
  – Processor starts a read operation to transfer data to memory
  – Disk interrupts when the transfer completes

Smart Controller Example
• Device contains embedded processor
• Offloads work from CPU
• Allows each device to operate independently
• Improves I/O and CPU performance
• Smart Device Example
  – Processor requests a read operation by specifying the location on the disk and the location in memory
  – Disk performs all steps of the operation and interrupts when the operation completes

Direct Memory Access (DMA)
• Important optimization
• Needed for high-speed I/O
• Device moves data across the bus to and from memory without using processor
• Requires smart controller

Buffer Chaining
• Handles multiple transfers without the processor
• Device given linked list of buffers
• Device hardware uses next buffer on list automatically
Scatter Read and Gather Write

- Special case of buffer chaining
- Large data transfer formed from separate blocks
- *Example:* to write a network packet, combine packet header from buffer 1 and packet data from buffer 2
- Eliminates application program from copying data into single, large buffer

Operation Chaining

- Further optimization for smart device
- Processor gives series of commands to device, sometimes called a channel program
- Device carries out successive commands automatically