VLSI

COMP375 Computer Architecture

Layers

- Applications
- Middleware – other CS classes
- High level languages
- Machine Language
- Microcode
- Logic circuits
- Gates
- Transistors
- Silicon structures

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- Applications
- Middleware
- High level languages
- Machine Language - earlier
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- Applications
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- Machine Language
- Microcode – later this semester
- Logic circuits
- Gates
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- Applications
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- Logic circuits – COMP370/ELEN327
- Gates
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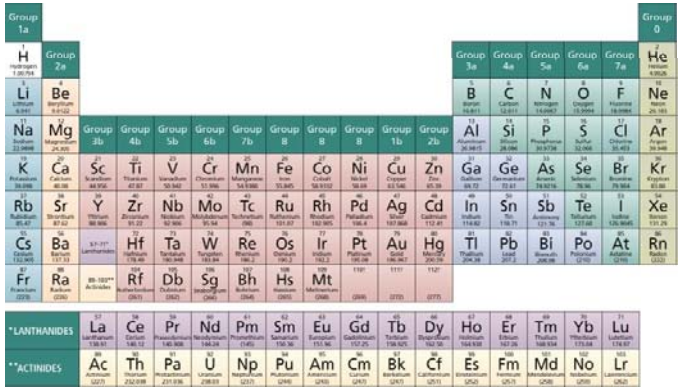
- Silicon structures

Layers

- Applications
- Middleware
- High level languages
- Machine Language
- Microcode
- Logic circuits
- Gates
- Transistors - Today
- Silicon structures

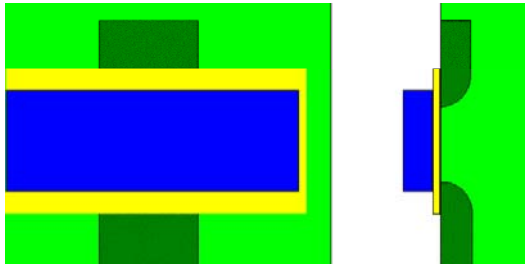
Periodic Table of Elements



Silicon

- Silicon has a valance of 4 and is in the middle of its row in the periodic table.
- Pure Silicon is a very poor conductor.
- Phosphorus has one more electron than Silicon. It is a **P** type dopant.
- Boron has one less electron than Silicon. It is an **N** type dopant.
- Adding just one part per million or less of a **P** dopant to silicon gives it extra electrons making it a good conductor.

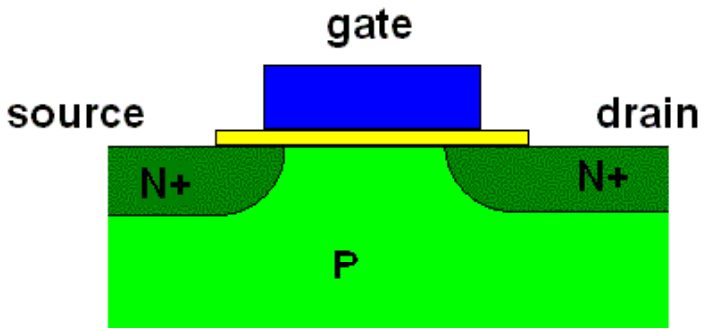
n-channel MOS transistor



Top View Side View

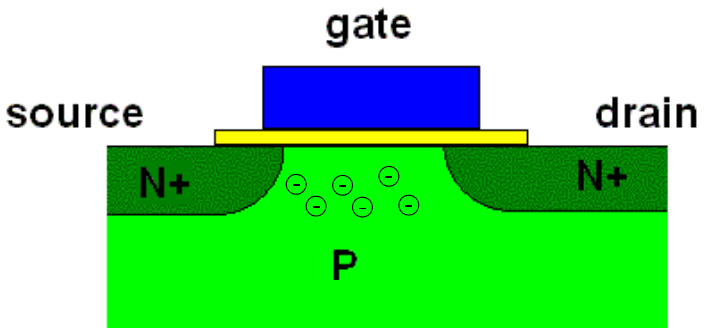
Metal	good conductor for gates
lightly P-doped silicon	normally poor conductor
heavily N-doped silicon	good conductor
Silicon Dioxide (glass)	insulator

NPN Transistor Operation



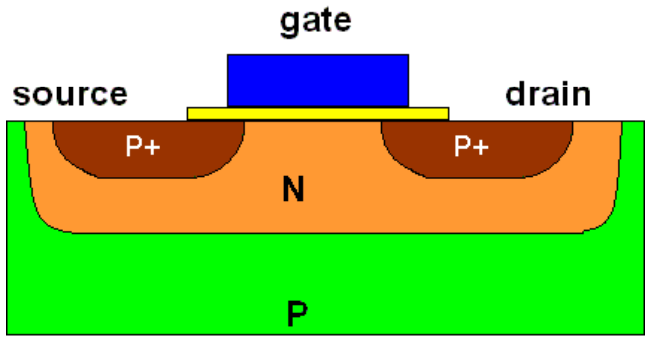
The low concentration P type silicon is a poor conductor. Therefore very little current flows from the source to the gate.

Transistor Operation



When positive voltage is applied to the gate, electrons are attracted to the gate. The presence of electrons allows current to flow between the source and drain.

PNP Transistor



Infusing a lot of N dopant in an area makes a well of N doped silicon. A PNP transistor can be built in the well.

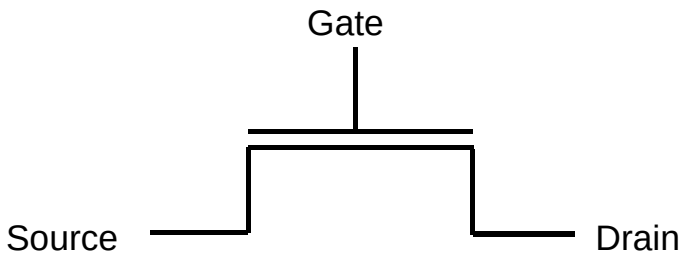
Complementary Operation

- **NPN** transistors conducts electricity between the source and drain when current is applied to the gate.
- **PNP** transistors conducts electricity between the source and drain when **no** current is applied to the gate. They stop conducting when current is applied to the gate.

CMOS

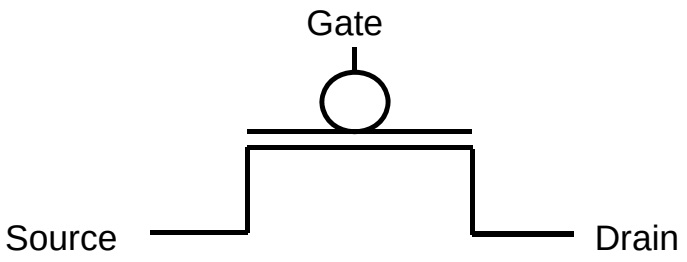
- **C**omplementary **M**etal **O**xide **S**emiconductor is a design technique using both NPN and PNP transistors.
- PNP transistors are used to connect the power to the output.
- NPN transistors are used to connect the ground to the output.
- The PNP and NPN circuits are exact logical inverses.

NPN Transistor Stick Diagram



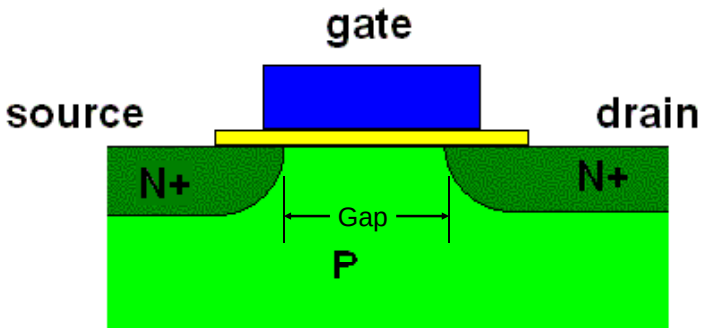
Conducts when the gate has current.

PNP Transistor Stick Diagram



Conducts when the gate does not have current.

Size Considerations

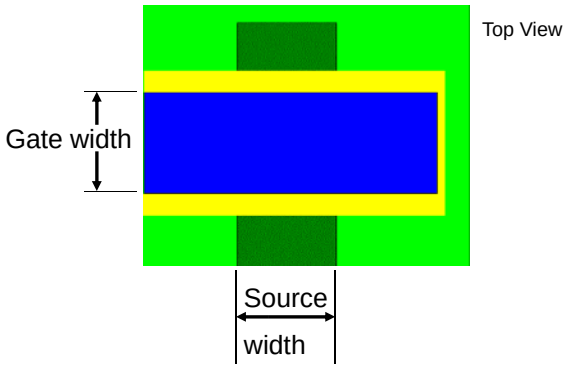


The smaller the region of P type silicon between the source and the drain, the faster the transistor.

Capacitance

- Capacitance is a circuit's ability to hold a charge.
- Greater capacitance increases the time required for a circuit to change voltage.
- Increasing the width of the transistor elements increases the capacitance.

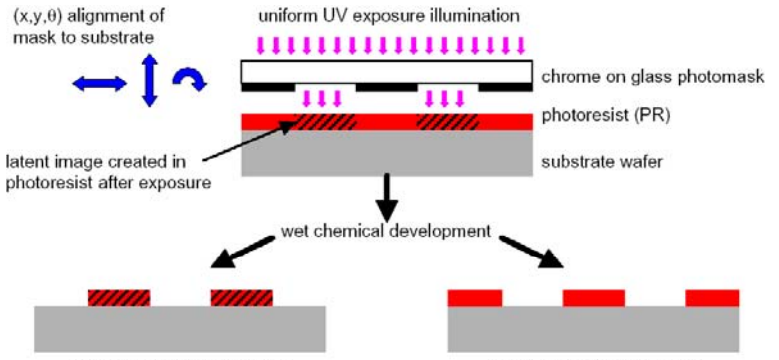
Capacitance Factors



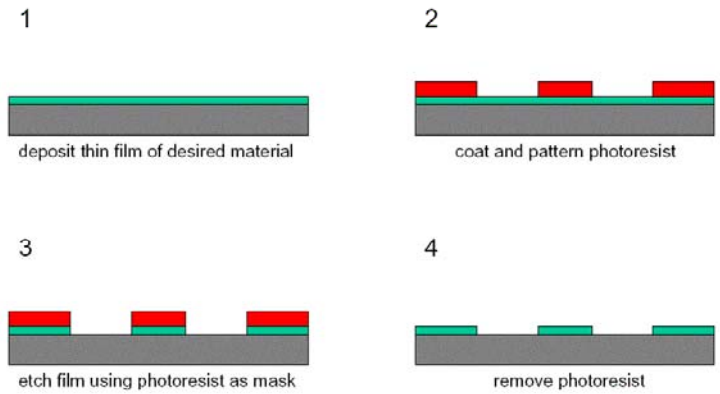
Very Large Scale Integration

- Transistors and the circuitry connecting them is built on a chip of silicon using **photolithography**.
- Millions of transistors can be manufactured on a single chip.

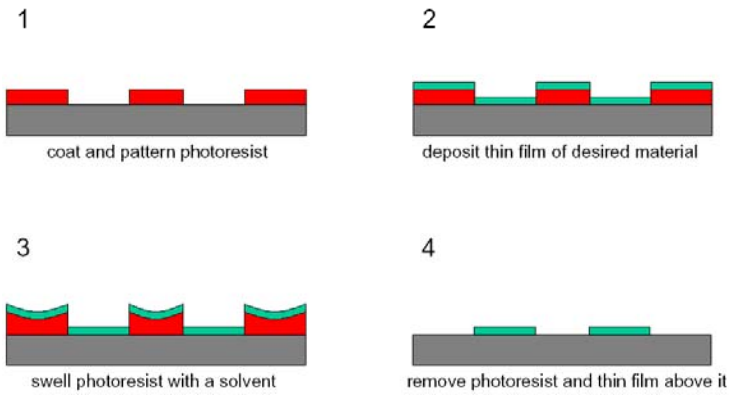
Photoresist



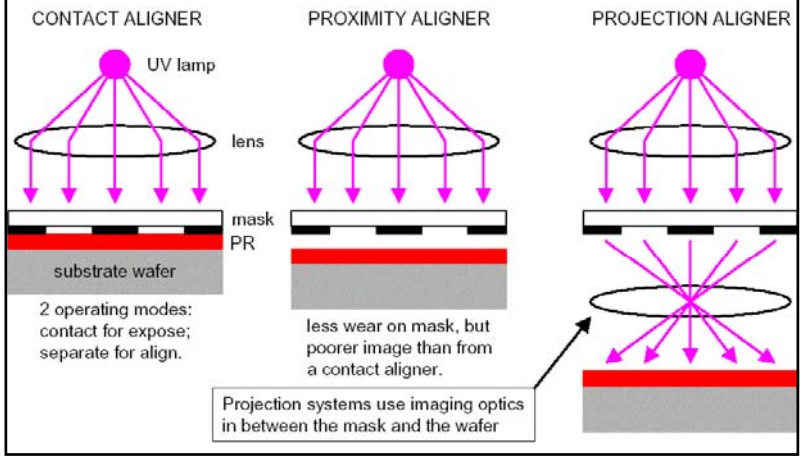
Photolithography Etching

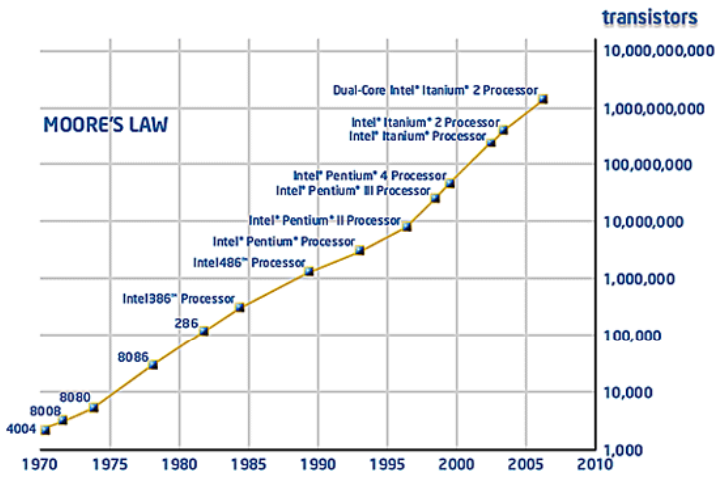


Photolithography Lift-off

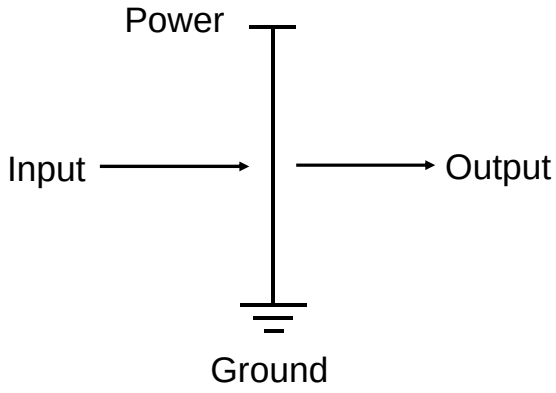


Projection Techniques



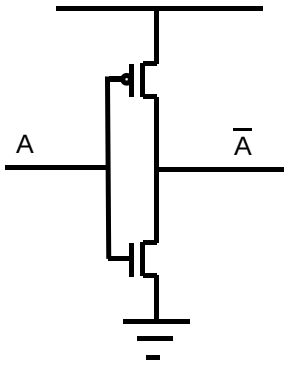


Logic Gate Components



Not Gate

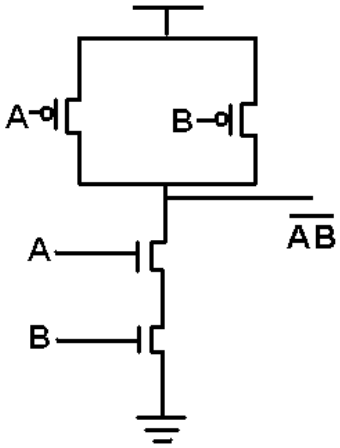
- When the input is 1 (current) the upper PNP transistor does not conduct. Power cannot flow to the output
- The lower NPN transistor does conduct. The output is connected to ground.
- When the input is 0 (no current) the upper PNP transistor can conduct power to the output.
- The lower NPN transistor does not connect the output to ground.



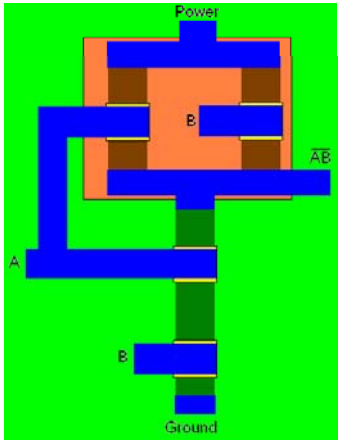
NAND Gate

- When either A or B is 0, the output is connected to power.
- When both A and B are one, the output is connected to ground.

A	B	output
0	0	1
0	1	1
1	0	1
1	1	0



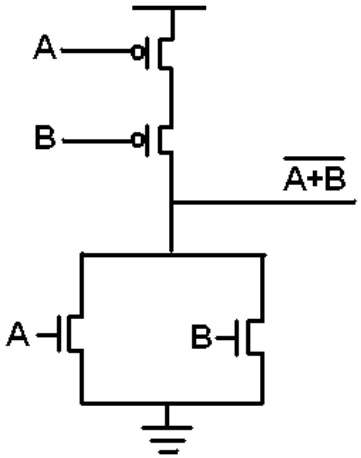
CMOS NAND transistors



NOR Gate

- When A & B are 0, the output is connected to power.
- When either A or B are one, the output is connected to ground.

A	B	output
0	0	1
0	1	0
1	0	0
1	1	0

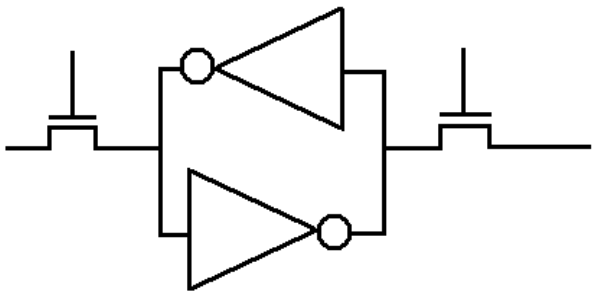


Shorts

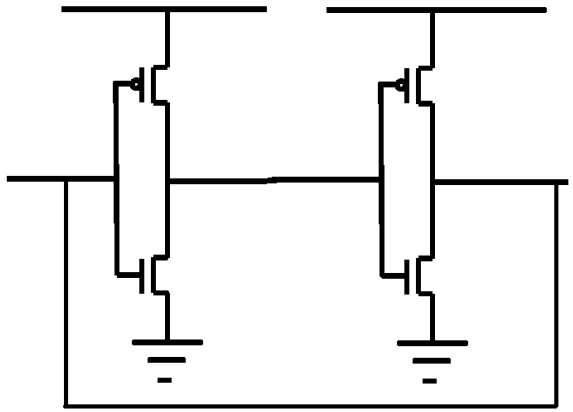
- It is important that no combination of inputs connects both the power and ground to the output. Power would flow from the power source to the ground creating a short and melting the chip.
- The output should always be connected to either the power or the ground. Otherwise the output will “float”.

Static RAM Cell

- Draw the below gate diagram using only transistors.



CMOS Static RAM Bit



More Complex Example

- Consider the carry out equation for a one bit adder

$$\overline{Cout} = AB + BC + AC$$

- The complement is

$$Cout = (\bar{A}+\bar{B})(\bar{B}+\bar{C})(\bar{A}+\bar{C})$$

CMOS Carry Circuit