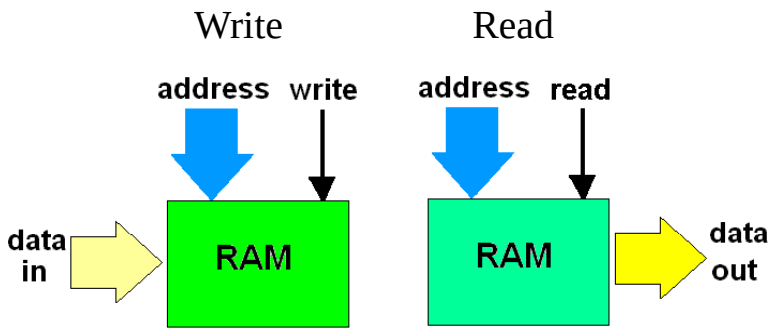
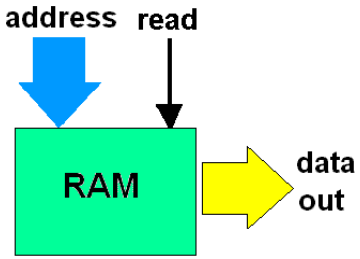
Memory Organization

COMP375 Computer Architecture and Organization

Simple Concept of Memory



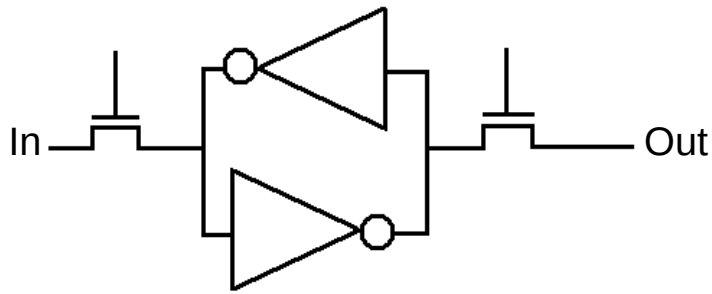
Address Length



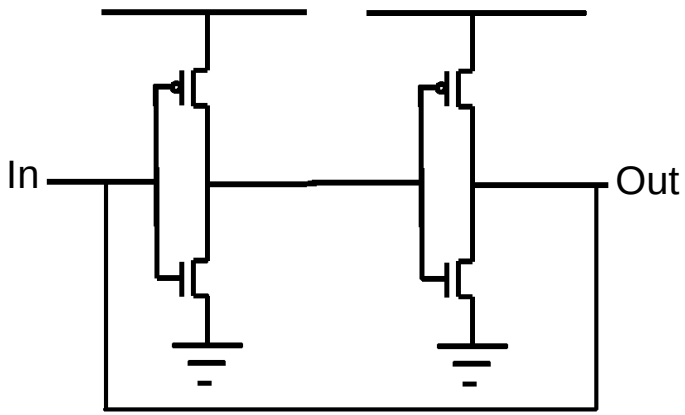
- If the RAM has N bytes, how many address lines are required?
- How many data out lines are required?

Static RAM Cell

- The SRAM bit is combined with input and output switches.

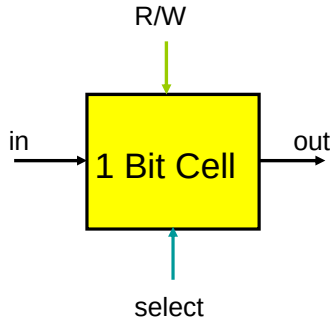


One SRAM Bit



1 Bit Cell

- Consider a one bit memory cell. It has:
  - input line for write
  - output line for read
  - R/W to indicate read or write
  - select to activate this cell



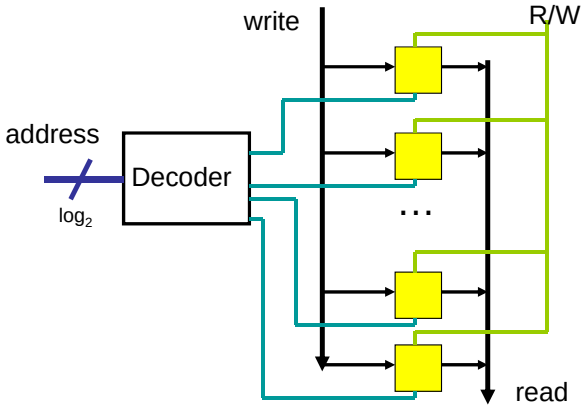
Combining Bits

- Since the computer has more than one bit of memory, we need to organize the bits into memory units.
- The number of bits in a memory unit depends on how many bits will fit.
- Bits can be grouped into units such as bytes or words.
- If you have X bits, you can divide it into N groups of M bits each where X = N * M

Usual Organization

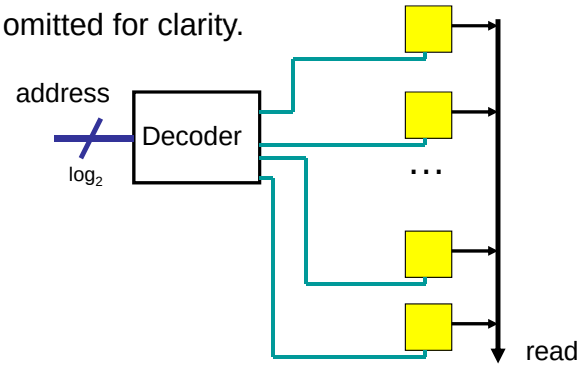
- DRAM chips are often created with small groups.
- A 1Mbit DRAM chip might load or store a single bit at a time.
- SRAM chips often input and output bytes or larger groups, such as words.

1 by N bit memory

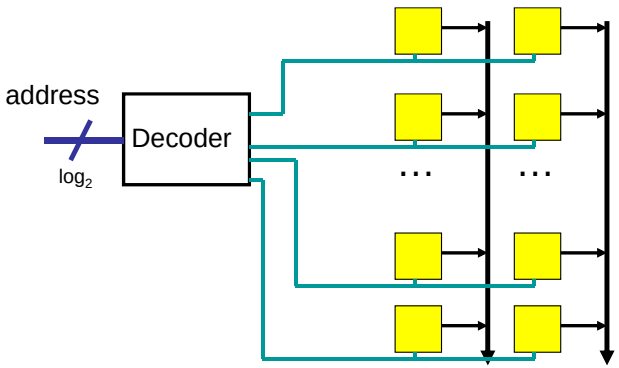


1 by N bit memory

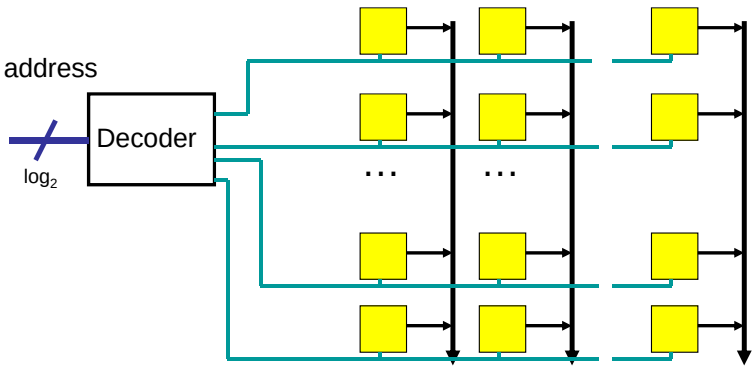
Write data and control lines have been omitted for clarity.



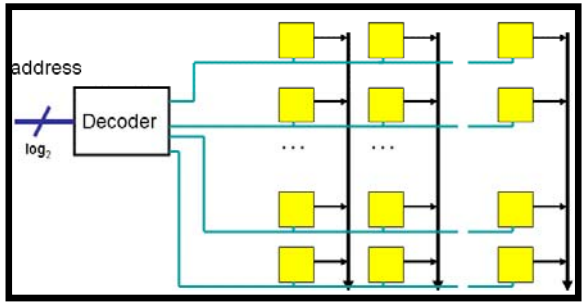
2 by N bit memory



M by N bit memory



Memory Modules



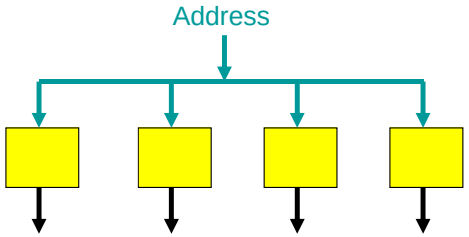
What inputs and outputs does this memory module have if it contains 16K bytes?

16K Byte Module Pins

- Addressing 16K bytes requires 14 pins
- Data input and output could be shared on 8 pins.
- Read/Write control is one pin
- Select is one pin
- The electronics may require additional pins for power, ground and clock.

Multiple Memory Modules

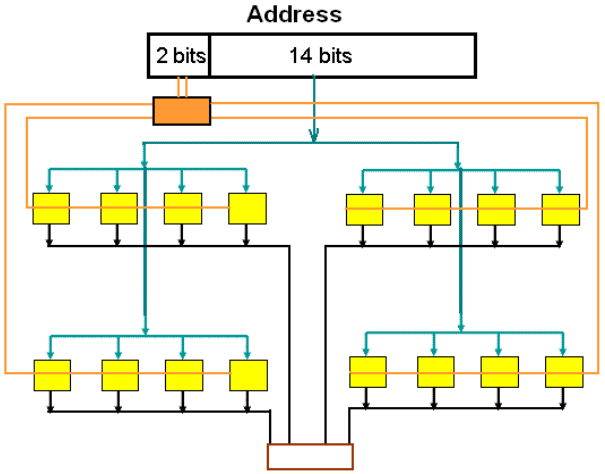
- Assume we want to combine our 16K byte modules to form 16K of 32 bit words.



Module Selection

- If you have X memory modules (where X is a power of 2), the upper $\log_2 X$ bits of the address can be used to select which memory module to use.

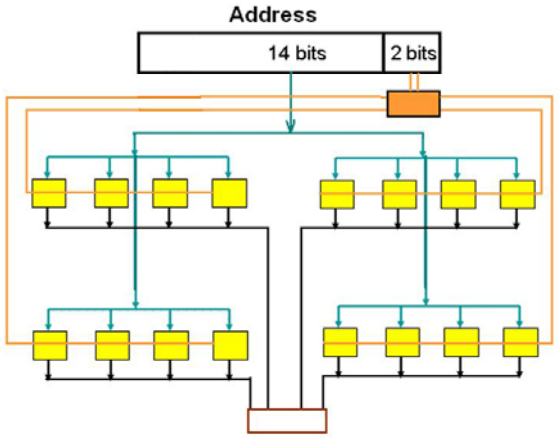
64K of 32 bit Words



Interleaved Memory

- The previous example used the upper bits of the address to select the memory module.
- Using the lower bits to select the memory module means that sequential addresses are in different modules.
- This can be advantageous if you are accessing sequential addresses and want to avoid memory access cycle delays.

64K of 32 bit Words Interleaved



Bus Width

- The width of the bus or the number of data wires in the bus, determines how many bits can be transferred from the RAM to the processor at one time.
- Many buses are 64 to 256 bits wide.
- The RAM needs to be designed to provide 64 to 256 bits at a time.